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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/627,924	07/28/2000	Joseph A Hook	FORE-73	3576

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EXAMINER

KADING, JOSHUA A

ART UNIT	PAPER NUMBER
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2661

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/627,924	Applicant(s) HOOK, JOSEPH A	
	Examiner Joshua Kading	Art Unit 2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 July 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 and 8-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6, 8 and 10-15 is/are rejected.
- 7) ☒ Claim(s) 9, 16, and 17 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
6) <input type="checkbox"/> Other: _____ |
|--|---|

DETAILED ACTION

Response to Amendment

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

5

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

10

Claims 1-6, and 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (U.S. Patent 5,870,625) in view of Yamanaka et al. (U.S. Patent 5,619,495).

15

In regard to claim 1, Chan discloses "a memory mechanism in which portions of packets...are stored" (col. 2, lines 29-30 show the transmission of packets in the network; figure 8, elements 220, 230 where 220 and 230 are buffers, or a memory mechanism, that store the incoming data as can be read in col. 12, lines 18-22, 29-32); and

20

"a mechanism for instituting changes to the memory mechanism while the memory mechanism is continuously operating on the portions of packets..." (figure 8, element 200 where the command buffer is the mechanism for instituting changes to the memory mechanism, and the memory mechanism can still operate on packets by

storing the incoming data into the buffers while the command buffer is instituting changes).

Chan lacks what Yamanka discloses, that is “a switch for a network (col. 9, lines 8-9)...”, “a plurality of fabrics” (figure 1, elements 13 and 14), and the packets are
5 “stripes” (figure 30 where the header processing unit separates the header from the data effectively turning them into fragments, or stripes).

It would have been obvious to one with ordinary skill in the art at the time of invention to include the “switch” with the “memory mechanism” and the “instituting mechanism” for the purpose of having the controller and the memory in the same unit.
10 The motivation for this being an increase in efficiency as the data has less distance to travel.

In regard to claim 2, Chan et al. and Yamanka et al. disclose the switch of claim 1. However, Chan et al. lacks “the memory mechanism that includes a plurality of
15 memory controllers.” Yamanka et al. however, further disclose “the memory mechanism that includes a plurality of memory controllers” (figure 30, elements 11₁ – 11_p, and 12₁ – 12_p; col. 2, line 8 where each memory mechanism includes or has a memory controller).
It would have been obvious to one with ordinary skill in the art at the time of invention to include the memory controllers with the switch of claim 1 for the same reasons and
20 motivation as in claim 1.

In regard to claim 3, Chan et al. and Yamanka et al. disclose the switch of claim 2. However, Yamanka et al. lack "the instituting mechanism includes a command buffer disposed in each memory controller in which changes to the memory controller are stored until the changes are implemented." Chan et al. however, further disclose "the instituting mechanism includes a command buffer disposed in each memory controller in which changes to the memory controller are stored until the changes are implemented" (figure 8, element 8 where the changes are stored in the wait buffer 210 until needed). It would have been obvious to one with ordinary skill in the art at the time of invention to include the command buffer with the switch of claim 2 for the same reasons and motivation as in claim 2.

In regard to claim 4, Chan et al. and Yamanka et al. disclose the switch of claim 3. However, Yamanka et al. lack "a fabric in which the memory mechanism and the instituting mechanism are disposed, and wherein the instituting mechanism includes an MCP (Module Control Processor) disposed in the fabric connected to the command buffer of each memory controller in the fabric, the MCP sends the changes to the buffer." Chan et al. however, further disclose "a fabric in which the memory mechanism and the instituting mechanism are disposed, and wherein the instituting mechanism includes an MCP disposed in the fabric connected to the command buffer of each memory controller in the fabric, the MCP sends the changes to the buffer" (figure 8, element 190 is the fabric in which the instituting mechanism and memory mechanism are disposed; figure 8, element 201 where 201 acts as the MCP by sending the

changes to be instituted (commands) to the wait buffer 210 and is clearly connected to the command buffer). It would have been obvious to one with ordinary skill in the art at the time of invention to include the MCP, the instituting mechanism, the memory mechanism all on the same fabric with the method of claim 3 for the same reasons and
5 motivation as claim 3.

In regard to claim 5, Chan et al. and Yamanka et al. disclose the switch of claim 4. However, Yamanka et al. lack "each memory controller institutes changes in its command buffer at a same logical clock cycle when the memory controller receives an
10 implementation signal." Chan et al. however, further disclose "each memory controller institutes changes in its command buffer at a same logical clock cycle when the memory controller receives an implementation signal" (figure 8, where it is shown in the figure that a command can come in on bus 160 at which point it can be stored in the wait
buffer 210, at the same time the execution buffer 203 can be instructing the memory
15 mechanism to perform a specific function, thus this can all be done during the same logical clock cycle). It would have been obvious to one with ordinary skill in the art at the time of invention to include the "same logical clock cycle" operations with the method of claim 4 to allow each memory controller to perform two tasks at once. The motivation being to increase efficiency in command execution.

20

In regard to claim 6, Chan et al. and Yamanka et al. disclose the switch of claim 5. However, Chan et al. lack "the fabric has an aggregator which receives the

implementation signal and sends it to the memory controllers.” Yamanka et al. however, further disclose “the fabric has an aggregator which receives the implementation signal and sends it to the memory controllers” (figure 29, element 130 where the multiplexer is the functional equivalent of an aggregator as per the specification, page 8, lines 12-15 and takes the input signals $1_1 - 1_n$ (as are in figure 30) aggregates them then sends them to the controller which can be taken to the buffer controller 15 of figure 30 which then sends these signals to the memory controllers $12_1 - 12_p$). It would have been obvious to one with ordinary skill in the art at the time of invention to include the aggregator with the method of claim 5 for the purpose of having the aggregator and the memory in the same unit. The motivation for this being an increase in efficiency as the data has less distance to travel.

Regarding claim 8, Chan and Yamanka disclose the switch of claim 6. However, Chan lacks what Yamanka further discloses, “a port card which receives the implementation signal from the network and sends the implementation signal to each fabric in the switch (figure 1, elements 10a1, 10a2, etc. are all port cards that receive signals, which include implementation signals, from the network, after they are received the implementation signals are sent to the buffer control 15 which uses them to produce the appropriate control signals to the fabrics 13 and 14, see col. 10, lines 64-col. 11, lines 1-37 with emphasis on the description of figure 2).” It would have been obvious to one with ordinary skill in the art to include the port card to carry the implementation

signal from the networks to the fabrics for the same reasons and motivation as in claim 6.

In regard to claim 10, Chan et al. disclose "a method...comprising:

5 receiving changes for the memory mechanism... at a buffer" (figure 8, elements 160, 200, 210 where the changes come in on bus 160 and are stored in buffer 210).

"implementing the changes to the memory mechanism when the memory mechanism receives an implementation signal while the memory mechanism continuously operates on the portions of the packets..." (figure 8, element 200 where
10 the command buffer is the mechanism for instituting changes to the memory mechanism, and the memory mechanism can still operate on packets by storing the incoming data into the buffers while the command buffer is instituting changes).

However, Chan lacks what Yamanaka discloses, that is "...switching packets...", "...a switch (col. 9, lines 8-9)...", "...a plurality of fabrics (figure 1, elements 13 and
15 14)...", "storing portions of packets as stripes in a memory mechanism (col. 10, lines 23-24 where the memory mechanism and instituting mechanism of Chan are functionally equivalent to the elements 11₁ and 12₁)", and the packets are "stripes" (figure 30 where the header processing unit separates the header from the data effectively turning them into fragments, or stripes).

20 It would have been obvious to one with ordinary skill in the art at the time of invention to include the "switch" with the "memory mechanism" and the "instituting mechanism" for the purpose of having the controller and the memory in the same unit.

The motivation for this being an increase in efficiency as the data has less distance to travel.

In regard to claim 11, Chan et al. and Yamanaka et al. disclose the method
5 according to claim 10. However, Yamanaka et al. lack "...the buffer includes a
command buffer and the receiving step includes the step of receiving changes for each
memory controller of each fabric at the command buffer." Chan et al. however, further
disclose "the buffer includes a command buffer and the receiving step includes the step
of receiving changes for each memory controller of each fabric at the command buffer"
10 (figure 8, element 8 where the changes are received and stored in the wait buffer 210
until needed). However, Chan lacks what Yamanaka further discloses, that is "the
memory mechanism includes a plurality of memory controllers with a memory controller
of the plurality of memory controllers disposed in each fabric (figure 30, elements 11₁ –
11_p, and 12₁ – 12_p; col. 2, line 8 where each memory mechanism includes or has a
15 memory controller)..." It would have been obvious to one with ordinary skill in the art at
the time of invention to include the command buffer and memory controllers with the
switch of claim 10 for the same reasons and motivation as in claim 10.

In regard to claim 12, Chan et al. and Yamanaka et al. disclose the method
20 according to claim 11. However, Yamanaka et al. lack "before the receiving step, there
is a step of sending the changes to each command buffer from a Module Control
Processor of each fabric." Chan et al. however, further disclose "before the receiving

step, there is a step of sending the changes to each command buffer from a Module Control Processor of each fabric" (figure 8, element 201 where 201 acts as the MCP by sending the changes to be instituted (commands) to the wait buffer 210 and it is clearly connected to the command buffer; it should also be noted that the sending step must
5 occur before the receiving step). It would have been obvious to one with ordinary skill in the art at the time of invention to include the sending step with the method of claim 11 for the same reasons and motivation as in claim 11.

In regard to claim 13, Chan et al. and Yamanaka et al. disclose the method
10 according to claim 12. However, Yamanaka et al. lack "the implementing step includes the step of implementing the changes to all the memory controllers of all the fabrics at a same logical clock cycle." Chan et al. however, further disclose "the implementing step includes the step of implementing the changes to all the memory controllers of all the fabrics at a same logical clock cycle" (figure 8, where it is shown in the figure that a
15 command can come in on bus 160 at which point it can be stored in the wait buffer 210, at the same time the execution buffer 203 can be instructing the memory mechanism to perform a specific function, thus this can all be done during the same logical clock cycle). It would have been obvious to one with ordinary skill in the art at the time of invention to include the "same logical clock cycle" operations with the method of claim
20 12 to allow each memory controller to perform two task at once. The motivation being to increase efficiency in command execution.

In regard to claim 14, Chan et al. and Yamanaka et al. disclose the method according to claim 13. However, Chan et al. and Yamanaka et al. lack explicitly "before the implementing step, there is [a] step of receiving the implementation signal at the switch in a receive message packet." However, it would have been obvious to "receive" the implementation signal in a receive message packet because in order to implement a command/step there must be some kind of message indicating what command/step that needs to be implemented. The only way to get this message is to receive it. It would have been obvious to one with ordinary skill in the art at the time of invention to include the receiving step with the method of claim 13 because there is no other way to obtain the implementation signal information. The motivation being to allow the system to accept implementation signals from a variety of sources.

In regard to claim 15, Chan et al. and Yamanaka et al. disclose the method according to claim 14. However, Chan et al. lack "the implementation [signal] receiving step includes the step of receiving the receive message packet at a port card of the switch." Yamanaka et al. however, further disclose "the implementation [signal] receiving step includes the step of receiving the receive message packet at a port card of the switch" (figure 30, elements 10₁ - 10_{an} where these elements act as port cards for the switching apparatus). It would have been obvious to one with ordinary skill in the art at the time of invention to include the port card with the method of claim 14 for the purpose of allowing signals access to the switch. The motivation being to have a switch that can accept signals.

Allowable Subject Matter

Claims 9, 16, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the

5 limitations of the base claim and any intervening claims.

Response to Arguments

Upon further consideration, the objection to claim 7 as originally presented is withdrawn, and the objection to claim 8 is also withdrawn.

10

Applicant's arguments with respect to claims 1-6, and 10-16 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the
15 examiner should be directed to Joshua Kading whose telephone number is (571) 272-3070. The examiner can normally be reached on M-F: 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 703-
20 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

- 5 For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joshua Kading
Examiner
Art Unit 2661

10 September 20, 2004



KENNETH VANDERPUYE
PRIMARY EXAMINER